CLAIM AMENDMENTS:

Please amend claims 1, 20 and 21, and cancel claims 10-19 and 27-36 as follows:

1. (Currently Amended) A three dimension (3D) polysilicon read only memory (ROM), at least comprising:

a silicon substrate;

an isolated silicon dioxide (SiO_2) layer, which is deposited on the silicon substrate;

a N-Type heavily doped (N+) polysilicon layer, which is deposited on the isolated SiO_2 layer and ~~is~~ further ~~defined~~ defines a plurality of parallel, separate word lines (WL);

a first oxide layer, which is filled in the space between the word lines;

a dielectric layer, which is deposited on the word lines and the first oxide layer;

a P-Type lightly doped (P-) polysilicon layer, which is deposited on the dielectric layer and ~~is~~ further ~~defined~~ defines a plurality of parallel, separate bit lines (BL), wherein the bit lines overlap the word lines, from a top view, to form a shape ~~approximately as~~ defines a cross;

at least a neck structure, which are individually formed between ~~the first polysilicon layer and the second polysilicon layer~~ the N-type heavily doped (N+) polysilicon layer and the P-type lightly doped (P-) polysilicon layer by ~~isotropy~~ isotropically etching the dielectric layer and using dilute hydrofluoric acid (HF); and

a second oxide layer, which is filled in the space between the bit lines and is on the word lines and the first oxide layer.

2. (Original) The 3D polysilicon ROM according to claim 1, wherein the N-Type heavily doped (N+) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

3. (Original) The 3D polysilicon ROM according to claim 1, wherein the P-Type lightly doped (P-) polysilicon layer is a sandwich structure of polysilicon/silicide/polysilicon.

4. (Original) The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are filled by high density plasma in the space between the word lines and between the bit lines, respectively.

5. (Original) The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of silicon nitride (Si_3N_4).

6. (Original) The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of Borophosphosilicate glass (BPSG).

7. (Original) The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of a polymer.

8. (Original) The 3D polysilicon ROM according to claim 1, wherein the first oxide layer and the second oxide layer are made of a low K material.

9. (Original) The 3D polysilicon ROM according to claim 1, wherein the material of the dielectric layer is selected from a group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2).

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Currently Amended) A 3D polysilicon ROM, at least comprising:

a silicon substrate;

depositing an isolated SiO_2 layer on the silicon substrate;

a plurality of parallel, separate word lines (WL), which are defined on the isolated SiO_2 layer;

a plurality of parallel, separate first bit line (BL) sections, which are formed on the word lines separately;

a plurality of parallel, separate dielectric sections, which are formed below the first BL sections one by one, each one being with respect to the first BL sections thereon and all being on the word lines;

at least a neck structure, which are individually formed for the dielectric sections with respect to the second bit lines thereon;

a first oxide layer, which is filled in the space between the word lines, in the space between the first BL sections, in the space between the dielectric sections, and is on the word lines;

a plurality of parallel, separate second bit lines, which are defined on the first BL sections and on the first oxide layer, wherein the second bit lines overlap the word lines, from a top view, to form a shape approximately as a cross and the second bit lines are electrically coupled to the first BL sections thereabout; and

a second oxide layer, which is filled in the space between the second bit lines and is on the first oxide layer over the word lines.

21. (Currently Amended) The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are filled by high density plasma in the space between the word lines and between the second bit lines, respectively.

22. (Original) The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of silicon nitride (Si_3N_4).

23. (Original) The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of Borophosphosilicate glass (BPSG).

24. (Original) The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of a polymer.

25. (Original) The 3D polysilicon ROM according to claim 20, wherein the first oxide layer and the second oxide layer are made of a low K material.

26. (Original) The 3D polysilicon ROM according to claim 20, wherein the material of the dielectric layer is selected from a group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2).

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)